CLAIMS

1. A semiconductor device comprising:

an n-type silicon carbide substrate (2) of a high impurity concentration;

an n-type silicon carbide layer (3) of a low impurity concentration disposed on the substrate;

a first n-type silicon carbide region (4) of a first impurity concentration disposed on a surface of said n-type silicon carbide layer of the low impurity concentration;

first p-type silicon carbide regions (5) disposed as adjoined to opposite sides of said first n-type silicon carbide region;

a second n-type silicon carbide region (6) of a second impurity concentration disposed selectively from a surface through an interior of said first p-type silicon carbide region at a position separated from said first n-type silicon carbide region;

polycrystalline silicon (7) having a metal or an impurity implanted therein and serving to short-circuit said first p-type silicon carbide region to said second n-type silicon carbide region;

a gate electrode (8) disposed in a surface part of said first p-type silicon carbide region through a gate insulating film (9); and

a third n-type silicon carbide region (10) of a third impurity concentration formed either between said first n-type silicon carbide region and the first p-type silicon carbide region below said gate electrode or between said second n-type silicon carbide region and the first p-type silicon carbide region below the gate electrode, or both, selectively from the surface through the interior of the first p-type silicon carbide region;

all components being individually formed in a vertical DMOS structure.

2. A semiconductor device according to claim 1, wherein said first p-type silicon carbide region (5) has a lower part formed as a second p-type silicon carbide region (5a) of a higher impurity concentration than said first p-type silicon carbide region.

3. A semiconductor device according to claim 1, further comprising an n-type silicon carbide region (10a) formed selectively from the surface through the interior of the

first p-type silicon carbide region below said gate electrode (8), wherein the n-type silicon carbide region has an impurity concentration sufficient to produce a buried channel region and the buried channel region is formed in a layer thickness 0.2 to 1.0 times a layer thickness of the second n-type silicon carbide region.

4. A semiconductor device according to claim 2, further comprising an n-type silicon carbide region (10a) formed selectively from the surface through the interior of the first p-type silicon carbide region below said gate electrode (8), wherein the n-type silicon carbide region has an impurity concentration sufficient to produce a buried channel region and the buried channel region is formed in a layer thickness 0.2 to 1.0 times a layer thickness of the second n-type silicon carbide region.

5. A semiconductor device according to claim 3 or claim 4, wherein said buried channel region has an impurity concentration in the range of $5 \times 10^{15}$ to $1 \times 10^{17}$ $cm^{-3}$.

6. A semiconductor device according to any one of claims 1 to 4, wherein said gate electrode (8) is formed of aluminum, an aluminum-containing alloy or molybdenum.

7. A semiconductor device according to any one of claims 1 to 4, wherein said gate electrode (8) is formed of a p-type polycrystalline silicon having boron implanted therein to a concentration in the range of $1 \times 10^{16}$ to $1 \times 10^{21}$ $cm^{-3}$.

8. A semiconductor device according to any one of claims 1 to 4, wherein said gate electrode (8) is formed of an n-type polycrystalline silicon having phosphorus or arsenic implanted therein to a concentration in the range of $1 \times 10^{16}$ to $1 \times 10^{21}$ $cm^{-3}$.

9. A semiconductor device according to any one of claims 1 to 4, further comprising a silicide film (13) deposited on said gate electrode (8), wherein the silicide film is formed of silicon and any one of tungsten, molybdenum and titanium.

10. A semiconductor device according to any one of claims 1 to 4, wherein said n-type silicon carbide layer (3) of a low impurity concentration is formed on a (11-20) face of the n-type substrate (2) of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

11. A semiconductor device according to claim 5, wherein said n-type silicon carbide layer (3) of a low impurity concentration is formed on a (11-20) face of the n-type substrate (2) of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

12. A semiconductor device according to claim 6, wherein said n-type silicon carbide layer (3) of a low impurity concentration is formed on a (11-20) face of the n-type substrate (2) of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

13. A semiconductor device according to claim 7, wherein said n-type silicon carbide layer (3) of a low impurity concentration is formed on a (11-20) face of the n-type substrate (2) of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

14. A semiconductor device according to claim 8, wherein said n-type silicon carbide layer (3) of a low impurity concentration is formed on a (11-20) face of the n-type substrate (2) of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

15. A semiconductor device according to claim 9, wherein said n-type silicon carbide layer (3) of a low impurity concentration is formed on a (11-20) face of the n-type substrate (2) of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

16. A semiconductor device according to any one of claims 1 to 4, wherein said n-type silicon carbide layer (3) of a low impurity concentration is formed on a (000-1) face of the n-type substrate (2) of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

17. A semiconductor device according to claim 5, wherein said n-type silicon carbide layer (3) of a low impurity concentration is formed on a (000-1) face of the n-type substrate (2) of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

18. A semiconductor device according to claim 6, wherein said n-type silicon carbide layer (3) of a low impurity concentration is formed on a (000-1) face of the n-type substrate (2) of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

19. A semiconductor device according to claim 7, wherein said n-type silicon carbide layer (3) of a low impurity concentration is formed on a (000-1) face of the n-type substrate (2) of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

20. A semiconductor device according to claim 8, wherein said n-type silicon carbide layer (3) of a low impurity concentration is formed on a (000-1) face of the n-type substrate (2) of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

21. A semiconductor device according to claim 9, wherein said n-type silicon carbide layer (3) of a low impurity concentration is formed on a (000-1) face of the n-type substrate (2) of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.